Starburst System Design: X-engine Packet Formats

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Contents

This is a work-in-progress! We can expect to add to this with time.

1 Introduction

The X-engine of Starburst produces a variety of accumulated products from the ROACH system. This document describes the binary format of these packets

2 Important note on packet sample order

Internally, the FPGA performs an FFT on the samples measured by the ADCs. Due to computational considerations, this FFT produes 8 streams (which is normal). The abnormal part, is that the final four out of eight streams of the FFT (each representing 1/8th of the sideband's frequency content, or 1/16th of the FPGA's total frequency content), are in REVERSE order. So, a packet containing frequency channels 4096-5119, actually releases those channels in the order ¡5119:-1:4096¿, just to give an example.

3 Packet format

Protocol: All packets will be sent using UDP. Each packet consists of a 16-byte header, followed by some number of 6-byte data points.

Each packet contains data which varies by frequency only; within a packet, data-type, accumulation start-time, polarization, etc are all held constant. Packets are transmitted in a burst once an accumulation has finished. The specific timings of this burst are fully configurable, although suitable default values will be provided.

Because re-ordering data on the FPGA is inconvienent, no real effort will be spent on re-ordering data in-FPGA. Spectra from the F-engine will be treated as streams of samples, all of which are essentially indistinguishable. Reordering will be performed on the PC.

This table describes the packet format:

Byte	Data name	Description
0	¡invalid data¿	
1	¡invalid data¿	
2	sec_cnt[0]	number of seconds since reset
3	sec_cnt[1]	
4	pkt_sec_cnt[0]	number of packets this second
5	pkt_sec_cnt[1]	
6	raw_pkt_cnt[0]	total number of packets
7	raw_pkt_cnt[1]	OR
8	raw_pkt_cnt[2]	number of FPGA clock cycles
9	raw_pkt_cnt[3]	since last 1pps signal
10	ramSel[0]	user configurable (per packet)
11	ramSel[1]	user configurable (per packet)
12	ramSel[2]	user configurable (per packet)
13	ramSel[3]	Contains packet ID
14	headerAll[0]	Custom 32 bits (shared for all packets)
15	headerAll[1]	
16	headerAll[2]	(headerAll[bit10 downto bit1]=acc_freq_mask)
17	headerAll[3]	(headerAll[bit0]=dcm_page_changed)
18	data[s0][b0]	MSB of 0th data sample
19	data[s0][b1]	next byte of 0th data sample
20	data[s0][b2]	⋮
21	data[s0][b3]	⋮
22	data[s0][b4]	⋮
23	data[s0][b5]	MSB of 1st data sample
24	data[s1][b0]	
25	data[s1][b1]	
⋮	⋮	⋮
6159	data[s1023][b4]	
6160	data[s1023][b5]	LSB of 1023rd data sample

3.1 Data types

Depending on the packet ID, the contents of data[sX][bY] mean different things:

3.1.1 SSB calibration packets ¡ID 0-63¿

SSB packets contain either the real or imaginary part of the cross-multiplication between a frequency chunk of the upper sideband (USB) or lower sideband (LSB). Each 6-byte sample is in two's complement.

Byte	Data name	Description
0	data[sX][b0]	SSB calibration (MSB)
1	data[sX][b1]	SSB calibration
2	data[sX][b2]	SSB calibration
3	data[sX][b3]	SSB calibration
4	data[sX][b4]	SSB calibration
5	data[sX][b5]	SSB calibration (LSB)

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Packet ID	Description	Real/Imag component
0	0-1023	Real
1	0-1023	Imag
2	2048-3071	Real
3	2048-3071	Imag
4	1024-2048	Real
5	1024-2048	Imag
6	3072-4095	Real
7	3072-4095	Imag
8	5120-6143	Real
9	5120-6143	Imag
10	6144-7167	Real
11	6144-7167	Imag
12	4096-5119	Real
13	4096-5119	Imag
14	7168-8191	Real
15	7168-8191	Imag

NOTE! THIS IS WRONG. buffer order is (addr 0:7) ===¿ (buf [6,2,7,3,4,0,1,5])

3.1.2 Autocorrelation (power) packets ¡ID 64-95¿

Autocorrelation packets are real-valued, 48 bit unsigned integers.

Byte	Data name	Description
0	data[sX][b0]	Autocorrelation Power (MSB)
1	data[sX][b1]	Autocorrelation Power
2	data[sX][b2]	Autocorrelation Power
3	data[sX][b3]	Autocorrelation Power
4	data[sX][b4]	Autocorrelation Power
5	data[sX][b5]	Autocorrelation Power (LSB)

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Packet ID	Channels	Sideband
64	0-1023	USB
65	2048-3071	USB
66	0-1023	LSB
67	2048-3071	LSB
68	1024-2047	USB
69	3072-4095	USB
70	1024-2047	LSB
71	3072-4095	LSB
72	4096-5119	USB
73	7168-8191	USB
74	4096-5119	LSB
75	7168-8191	LSB
76	5120-6143	USB
77	6144-7167	USB
78	5120-6143	LSB
79	6144-7167	LSB

3.1.3 Autocorrelation (fourth moment) packets ¡ID 96-127¿

Fourth moment values need 96 bits (twice as many as autocorrelation power values. These are produced in two separate packets. To recover the true fourth-moment estimate, compute $2^{48}F_{upper} + F_{lower}$

Byte	Data name	Description
0	data[sX][b0]	Fourth moment component (MSB)
1	data[sX][b1]	Fourth moment component
2	data[sX][b2]	Fourth moment component
3	data[sX][b3]	Fourth moment component
4	data[sX][b4]	Fourth moment component
5	data[sX][b5]	Fourth moment component (LSB)

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Packet ID	Channels	Sideband	Bits
96	0-1023	USB	upper 48
97	0-1023	USB	lower 48
98	2048-3071	USB	upper 48
99	2048-3071	USB	lower 48
100	0-1023	LSB	upper 48
101	0-1023	LSB	lower 48
102	2048-3071	LSB	upper 48
103	2048-3071	LSB	lower 48
104	1024-2047	USB	upper 48
105	1024-2047	USB	lower 48
106	3072-4095	USB	upper 48
107	3072-4095	USB	lower 48
108	1024-2047	LSB	upper 48
109	1024-2047	LSB	lower 48
110	3072-4095	LSB	upper 48
111	3072-4095	LSB	lower 48
112	4096-5119	USB	upper 48
113	4096-5119	USB	lower 48
114	7168-8191	USB	upper 48
115	7168-8191	USB	lower 48
116	4096-5119	LSB	upper 48
117	4096-5119	LSB	lower 48
118	7168-8191	LSB	upper 48
119	7168-8191	LSB	lower 48
120	5120-6143	USB	upper 48
121	5120-6143	USB	lower 48
122	6144-7167	USB	upper 48
123	6144-7167	USB	lower 48
124	5120-6143	LSB	upper 48
125	5120-6143	LSB	lower 48
126	6144-7167	LSB	upper 48
127	6144-7167	LSB	lower 48

3.1.4 Cross-multiply packets ¡ID 128-191¿

Because of the small input bit widths, we do not need as many bits for the cross-multiplies; they are contained within a single packet. So, two 24-bit, two's complement signed integers.

Because each ROACH processes a different chunk of the spectrum, the specific frequencies which each packet represents will differ from ROACH to ROACH.

Byte	Data name	Description
0	data[sX][b0]	Cross-multiply sample [Real] (MSB)
1	data[sX][b1]	Cross-multiply sample [Real]
2	data[sX][b2]	Cross-multiply sample [Real] (LSB)
3	data[sX][b3]	Cross-multiply sample [Imag] (MSB)
4	data[sX][b4]	Cross-multiply sample [Imag]
5	data[sX][b5]	Cross-multiply sample [Imag] (LSB)

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Packet ID	Source1 (TGE port)	Source1 (upper/lower)	Source2 (TGE port)	Source2 (upper/lower)
128	1	upper	3	upper
129	1	upper	5	upper
130	1	upper	7	upper
131	3	upper	5	upper
132	3	upper	7	upper
133	5	upper	7	upper
134				
135				
136	1	lower	3	lower
137	1	lower	5	lower
138	1	lower	7	lower
139	3	lower	5	lower
140	3	lower	7	lower
141	5	lower	7	lower
142				
143				
144	2	upper	4	upper
145	2	upper	6	upper
146	2	upper	8	upper
147	4	upper	6	upper
148	4	upper	8	upper
149	6	upper	8	upper
150				
151				
152	2	lower	4	lower
153	2	lower	6	lower
154	2	lower	8	lower
155	4	lower	6	lower
156	4	lower	8	lower
157	6	lower	8	lower
158				
159				

3.1.5 Histogram packets ¡ID 192,193¿

Each physical ADC chip has four cores. These cores are internally interleaved under-the-hood. The histogram module produces a separate histogram for each core. The codes produced descrbe the number of samples which contained a specific ADC code during the last integration.

Errata for the histogram module are as follows:

1. Unlike other modules of the Starburst correlator, the histogram module halts production of the histogram estimate when data is being read out for transmission. If this is late in the list-of-packets, the data contained in the histogram may differ significantly from the spectra in other accumulation products. For this reason, it is recommended that the user list the histogram products as the first outputs in each accumulation dump.

2. For efficiency's sake, only each fifth (confirm ratio) sample is processed into a histogram readout.

Each data point is a 48-bit unsigned integer.

Byte	Data name	Description
0	data[sX][b0]	Histogram value (MSB)
1	data[sX][b1]	Histogram value
2	data[sX][b2]	Histogram value
3	data[sX][b3]	Histogram value
4	data[sX][b4]	Histogram value
5	data[sX][b5]	Histogram value (LSB)

Sample	Data name	Description
0	data[s0][bX]	ADC[X][core=0][code=0]
1	data[s1][bX]	ADC[X][core=0][code=1]
2	data[s2][bX]	ADC[X][core=0][code=2]
⋮	⋮	⋮
255	data[s255][bX]	ADC[X][core=0][code=255]
256	data[s256][bX]	ADC[X][core=1][code=0]
257	data[s257][bX]	ADC[X][core=1][code=1]
⋮	⋮	⋮
511	data[s511][bX]	ADC[X][core=1][code=255]
512	data[s512][bX]	ADC[X][core=2][code=0]
513	data[s513][bX]	ADC[X][core=2][code=1]
⋮	⋮	⋮
1022	data[s1022][bX]	ADC[X][core=3][code=254]
1023	data[s1023][bX]	ADC[X][core=3][code=255]

4 Configuring the Starburst Packet Engine

All of the above data products are computed on every accumulation. Any subset of these potential packets can be transmitted via 1gbe through the appropriate setting of starburst registers. There are two important considerations when setting this configuration:

1. All packets from the current accumulation must be fully transmitted before the next acumulation is finished

2. Each packet must be fully (mostly) transmitted before starting the next packet.