Starburst System Design: Packet Formats

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March 4, 2016

Contents

This is a work-in-progress! We can expect to add to this with time.

1   Introduction

The purpose of the F-engine is to produce spectra at full-duty-cycle from its ADCs. The F-engine also performs sideband-separation, synchronization and bandpass-levelling on the data. Afterwords, the data is sent via 10-gigabit-ethernet to the X-engine in order to be correlated before being output to a host computer. This document is meant to define the contents of each "packet" which is to be transmitted between machines. A different packet format will be used for both the F- and X-engine.

2   F-Engine

Protocol: All packets will be sent using UDP. Because all of our links are point-to-point, there is no serious fear of dropped packets.

Because re-ordering data on the FPGA is inconvenient, no real effort will be spent on re-ordering data in-FPGA. Spectra from the F-engine will be treated as streams of samples, all of which are essentially indistinguishable. Reordering will be performed on the PC, if needed.

The first 128 bits sent are to be header information

Byte	Data name	Description
0	pkt_sec_cnt[0]	number of packets this second
1	pkt_sec_cnt[1]	(note! uppermost bit is always 0)
2	sec_cnt[0]	number of seconds since reset
3	sec_cnt[1]	
4	raw_pkt_cnt[0]	total number of packets
5	raw_pkt_cnt[1]	OR
6	raw_pkt_cnt[2]	number of FPGA clock cycles
7	raw_pkt_cnt[3]	since last 1pps signal
8	headerUpper[0]	Custom 32 bits (shared for all packets)
9	headerUpper[1]	
10	headerUpper[2]	
11	headerUpper[3]	
12	headerLower[0]	Custom 32 bits (shared for all packets)
13	headerLower[1]	
14	headerLower[2]	
15	headerLower[3]	
16	data[s0][b0]	MSB of 0th data sample
17	data[s0][b1]	next byte of 0th data sample
18	data[s0][b2]	⋮
19	data[s0][b3]	⋮
20	data[s0][b4]	⋮
21	data[s0][b5]	MSB of 1st data sample
22	data[s1][b0]	
23	data[s1][b1]	
⋮	⋮	⋮
6159	data[s1023][b4]	
6160	data[s1023][b5]	LSB of 1023rd data sample